IMPLEMENTATION OF IRREVERSIBLE AND REVERSIBLE CIRCUITS USING LAYERED T METHODOLOGY TO DESIGN HIGH PERFORMANCE DIGITAL LOGIC CIRCUITS BASED ON QUANTUM CELLULAR AUTOMATA (QCA)

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Abstract

In the last two years, CMOS-based semiconductor technology has experienced two simultaneous discontinuities. The semiconductor industry addresses the physical constraints of current semiconductor materials and the impending end of Moore's forecast. Scientists have been compelled to rethink innovative computing devices and architectures as a consequence of these obstacles. The latest edition of the International Roadmap for Devices and Systems reveals that the semiconductor industry is now combining *More Moore*, *More than Moore*, and *Beyond CMOS* to explore the possibilities towards the alternatives like carbon nanotube, spintronics, molecular electronics, and quantum-dot cellular automata. Some significant works on quantum-dot cellular automata (QCA), including experimental fabrication to the device characterisation, show better prospects in this field. QCA leads the processor-based computation in the direction where device functionality gets more priority than the physical specifications. This nanotechnology-based paradigm's fast working speed, extremely low energy dissipation, and ultra-high packing density make it incredibly appealing. The architecture of QCA-based computing operates on quantum-mechanical tunnelling between the electrons rather than the conventional voltage and current flow in the circuit.

Several logic gates have been introduced in QCA like Majority Voter (MV), And-Or-Inverter (AOI), Universal QCA (UQCAL), FNZ and Layered T logic. The Layered T (LT) Gate excels in the QCA implementation of the digital logic design paradigm since it operates with a stable and physically realisable fixed polarised cell. The LT logic reduction methodology is utilised in combinational and sequential computational blocks of a nano processor like an adder, subtractor, multiplexer, demultiplexer, multiplier, flip-flop, counter, register, and memory and in developing QCA designs of reversible circuits.

In this dissertation, the different prospects of LT Gate have been explored since it realises universal NAND/NOR based logic as the elementary level functionality. The behavioural logic synthesis, characterisation, defect and fault-tolerant performance of the LT gate is provided. The reproducibility, repeatability, scalability and flexibility of LT gate are verified through the realisation of *standard functions*, generic combinational and sequential logic circuits, and memory designs.

Furthermore, the notion of LT logic is extended in the reversible circuits and *Reversible Benchmark* design. This dissertation provides the proper guidelines to implement QCA counterparts of reversible circuits and vice versa.

The multilayer QCA fabrications have many issues to overcome the impacts of defects, faults and fabrication metrics on circuit functionality. The robustness of the LT gate is investigated by examining the *fabrication-based* and *logic circuit design based* QCA design parameters. The *fabrication-based* metrics analyse the effect of variation of layer separation, the impact of changing Radius of Effect (RoE), the change of consecutive cell spacing, cell dimensions and dot diameter on device-level functionality. In contrast, *logic circuit design* metrics are O-Cost, effective area, delay. Moreover, *logic circuit design based* QCA metrics validate the functionality of the entire QCA layout in terms of irreversible power dissipation (IPD), complexity and Cost Function ($Cost_{\alpha}$).

This dissertation provides an insight into the irreversible and reversible circuit design using LT logic reduction methodology. Additionally, a detailed technical background is provided on the designability of the proposed structures. Intricate details of design metrics and crossovers are also explained for the generated QCA layouts. The higher order irreversible and reversible components of a nano-processor are exhibited in most case studies with the supporting figures and output diagrams. The proposed layouts are compared with the existing designs, and the improvements are provided in detail.